SYSTEM MINIATURIZATION VIA HETEROGENEOUS INTEGRATION OF ELECTRONIC DEVICES FOR DEEP SPACE MISSIONS L. Del Castillo, D. V. Schatzel, R. W. Graber and A. Mottiwala, All authors affiliated with Jet Propulsion Laboratory, California Institute of Technology, 4800 Oak Grove Drive, Pasadena, California 91109.

Introduction: The scientific devices designed for each of the Outer Planets Program focuses will likely be groundbreaking not only with respect to their scientific role but also regarding the electronics required to perform such investigations. In the past, the performance of packaged electronics was limited by the components themselves, with minimal influence of the packaging technology. However, the rapid development of integrated circuit technology has drastically increased the role of packaging technology in the ultimate performance of devices. If not carefully considered in the overall design, the packaging may become the limiting factor in the operation of the system.

Discussion: The increased functionality and performance of integrated circuits drastically increased the required number of input/output connections, requiring larger die sizes to accommodate the traditional wirebonding interconnection method. Such increases in die size led to larger body sizes and longer wire lengths for bonding the die pads to the package, ultimately resulting in decreased electrical performance. Controlled collapse chip connection technology (flip chip technology), which has been successfully used by IBM for over 25 years and has been proven to be highly reliable in the field, provides a viable solution. Area array flip chip technology can provide a 30-50% decrease in die size, while allowing a higher number of input/output connections.[1] The use of such technology would both reduce the size of electronic devices and improve the performance. Since the design of the package is determined by the design and operating conditions of the device, however, commercial electronics manufacturers can only provide a starting point for the technology required for electronic systems intended for outer solar system missions. In addition to the traditional factors considered in electronic packaging, such as manufacturability, reliability, serviceability, size, weight, signal integrity, mechanical stability, power consumption, and heat dissipation problems, the present program offers unique challenges regarding the environment and conditions to be experienced by the devices. Size and mass must be minimized beyond the requirements of standard electronics, while obtaining 100% reliability due to the inability to repair devices.

To that end, the objective of the present project is to develop and optimize the interconnection technologies that are used to integrate active devices (microprocessors), passive integrated devices (capacitors, inductors, resistors), and Micro Electro-Mechanical Systems (microgyros, sensors) into a heterogeneous package configuration that can be validated for space flight application. The interconnection development method will concentrate on the attachment interfaces that will allow the integration of an electrical system. Development efforts will include different pad metallurgies and connection materials as well as developing mechanical models to perform stress analysis and identify connection failure modes. To verify reliability, the fabricated packages will be subjected to potential mission environments, such as the extreme temperatures of Neptune and the high radiation of Europa. The deliverable output of the development efforts will incorporate an implementation requirements document that includes manufacturing and design guidelines to be used as an aid and reference for future electrical circuits using advanced integrated passive devices. Therefore, as an integral part of the infrastructure and multi-mission technologies focus, the presently proposed project will enhance outer solar system exploration for each of the missions.

References: [1] R. N. Master (1997) *APEX 2001,* AT6 21-AT6 27.

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